Amendments to the Specification:

Please replace the paragraph beginning at line 17, page 5, with the following:

A clock generator 142 provides the basic clocking signal 148 that drives buffer logic ~~211~~ 141 and thereby establishes the operating frequency of network link 211. In the depicted embodiment, clock generator 142 is capable of providing clocking signal 148 at various frequencies controlled by the settings in a clock register 146. Clock register 146 is under the programmable control of processor 140. A memory 143 is accessible to processor 140 and buffer logic 141. Memory 140 may include volatile storage such as a conventional dynamic or static random access memory (DRAM or SRAM) array as well as persistent or non-volatile storage such as a flash memory card or other form of electrically erasable programmable read only memory (EEPROM).